

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Takaki YOSHIDA et al.

Serial No.: New Application

Group Art Unit:

Filed: October 27, 2000

Examiner:

For: FAULT DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR  
INTEGRATED CIRCUIT



INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO-1449. Copies of each of the references listed on Form PTO-1449 are attached.

The above information is presented so that the Patent and Trademark Office may, in the first instance, determine any materiality thereof to the claimed invention. See 37 C.F.R. 1.104(a) and 1.106(b) concerning the PTO duty to consider and use any such information. It is respectfully requested that the information be expressly considered during the prosecution of this

*Signature*  
1-17-01

application, and that these references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

October 27, 2000

Date

RWP/ch

Attorney Docket No.: YMOR:186

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